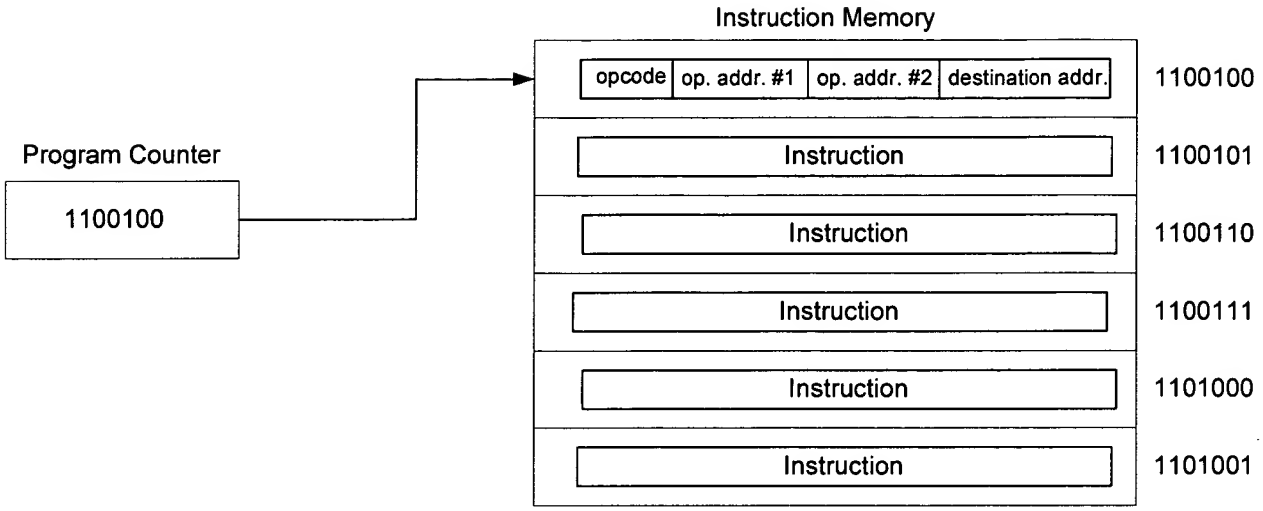

The diagram above shows a program counter and an instruction memory that stores a plurality of instructions. The value of the program counter is an instruction address that indicates the address in memory of the next instruction to be fetched. In the example above, the value of the program counter is "1100100." Thus, the next instruction to be fetched is the instruction stored at the memory address "1100100." That is, the value "1100100" is an instruction address. As shown in the diagram above, the instruction stored at instruction address "1100100" includes an opcode, which defines what operation is to be performed, two operand addresses, which indicate the memory locations of the operands on which the operation is to be performed, and a destination address, which indicates the memory location of the result. Thus, the instruction stored at memory address "1100100" may be an add instruction as shown in the diagram below.

opcode	op. addr. #1	op. addr. #2	destination addr.
ADD	110010	111010	1000010

That is, the opcode of the instruction indicates that an add operation is to be performed. The location of the operands to be added in the add operation is also indicated in the instruction. That is, the first operand is stored at memory address "110010" and the second operand is stored

at memory address "111010." The instruction also indicates the address of the memory location where the result of the add operation is to be stored (i.e., memory address "1000010").

Circello discloses that instruction addresses are provided from the processor core 9 to the debug module 10, **but does not disclose or suggest that an operand address is provided from the processor core 9 to the debug module 10.**

B. The Examiner's Response

In response to this example, the Office Action asserts that "the depiction shown in Applicants' remarks is only one of many instruction structure seen in binary code executed by a microprocessor. In the case of Applicants' depiction it is only a case of **indirect address** where in many program instructions the operands might be located by address references in an instruction content. However, the question is why Applicants do not depict an ADD address in which the **operand values are directly after an opcode**...(emphasis in original)." *See* Office Action, page 3, lines 1-7.

The Office Action appears to assert that, in Circello, operands may be located in an instruction and that the address of the instruction is, therefore, the operand address.

C. Circello Does Not Disclose That Operands Are Located In Instructions

Applicants respectfully disagree that operands may be located in an instruction. Further, Circello simply does not disclose that operands may be located in instructions. As stated in MPEP §2131, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Nowhere does Circello disclose that operands may be located in instructions. This is simply not disclosed in the reference. The Examiner has cited no reference that such an architecture even exists, let alone that this purported architecture is used in the system of Circello.

Thus, the rejection is improper because Circello does not disclose that operands may be located in instructions or that an instruction address may also be the address of an operand of that instruction. If the rejection is to be maintained, it is respectfully requested that the Examiner provide evidence that purported architecture described in the Office Action (i.e., an architecture

wherein operand values are located in instructions): 1) exists; and 2) is used by the system of Circello.

Thus, Circello does not disclose or suggest that the processor is configured to transmit, through a communication link, "a plurality of bit values, each representing a state of an operation in the processor, including at least an operand address that indicates a memory location at which an operand value is stored," as recited in independent claim 1. Therefore, claim 1 patentably distinguishes over Circello. Accordingly, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. §102(b).

Claims 2-20 and 61 depend from claim 1 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of these claims under 35 U.S.C. §102(b) be withdrawn.

Claim 21 is directed to a microcomputer comprising, "a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of: an operand address that indicates a memory location at which an operand value is stored." As should be clear from the discussion above, Circello does not disclose or suggest a processor that is configured to transmit an operand address to the debug circuit. Thus, claim 21 patentably distinguishes over Circello. Accordingly, it is respectfully requested that the rejection of claim 21 under 35 U.S.C. §102(b).

Claim 62 depends from claim 61 and is patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of claim 21 under 35 U.S.C. §102(b) be withdrawn.

Claim 22 is directed to a microcomputer comprising, "means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored." As should be clear from the discussion above, Circello does not disclose or suggest a transmitting an operand address to the debug circuit. Thus, claim 22 patentably distinguishes over Circello. Accordingly, it is respectfully requested that the rejection of claim 22 under 35 U.S.C. §102(b).

Claims 23-41 and 63 depend from claim 22 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of these claims under 35 U.S.C. §102(b) be withdrawn.

Claim 42 is directed to a method for transferring information between a processor and a debug circuit over a communication link. The method comprises, "transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored." As should be clear from the discussion above, Circello does not disclose or suggest a transmitting an operand address to the debug circuit. Thus, claim 42 patentably distinguishes over Circello. Accordingly, it is respectfully requested that the rejection of claim 42 under 35 U.S.C. §102(b).

Claims 43-60 and 64 depend from claim 42 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of these claims under 35 U.S.C. §102(b) be withdrawn.

CONCLUSION

In view of the foregoing remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

David Alan Edwards, et al., Applicants

By: _____

James H. Morris, Reg. No.: 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Telephone: (617) 720-3500

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